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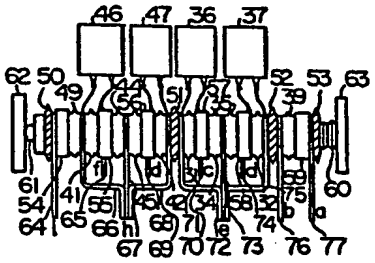
(54) **Gate turn-off thyristor stack.**

(57) A GTO thyristor stack comprises a pair of GTO thyristors (31, 32; 41, 42) in parallel connection and a pair of diodes (34, 35; 44, 45) in anti-parallel connection therewith. The elements in one of the GTO thyristor pair and the diode pair are located in the middle of the stack structure and sandwiched by the elements in the other with all the elements stacked in electrical connection. The stack structure is clamped by a pair of clamper members (62, 63).

FIG. 3



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GATE TURN-OFF THYRISTOR STACK

This invention relates to an improvement in a gate turn-off (hereinafter referred to as GTO) thyristor stack comprised of GTO thyristors in parallel connection.

Recently, the GTO thyristor having self-turn off capability has been gaining its capacity, and its application to power conversion devices such as converters, inverters, choppers or cyclo-converters has been extending. However, the GTO thyristor has inherent difficulties in increasing its current capacity and it is general to use two GTO thyristors in parallel connection.

Another problem encountered in a circuit utilizing GTO thyristors is that wiring inductance must be minimized to assure self-turn off function of the GTO thyristor. As the capacity increases, so this problem becomes difficult to solve.

This accounts for the fact that when the GTO thyristors are used, for example, to construct a PWM (pulse width modulation) inverter adapted to drive an induction motor, the distance between these GTO thyristors in parallel connection and circuit parts associated therewith must be so designed as to be minimized.

It is therefore an object of this invention to provide a GTO thyristor stack capable of r ducing

in size two GTO thyristor circuits in parallel connection each having a GTO thyristor and a diode in anti-parallel connection therewith, thereby minimizing wiring inductance of the circuits.

According to this invention, there is provided a gate turn-off thyristor stack comprising a pair of flat type gate turn-off thyristor elements to be connected in parallel with each other and a pair of flat type diode elements to be connected in direct parallel with the respective gate turn-off thyristor elements, wherein all the elements are stacked with electrical connection between the adjacent elements so that the elements in one of the gate turn-off thyristor element pair and the diode element pair are located opposite to each other at the middle of the stack structure and are sandwiched by the associated elements in the other pair which are provided on both sides of the stack structure, respectively, and the resulting stack structure is clamped by a pair of clamper members.

With this construction, the GTO thyristor elements and the associated diode elements can be stacked without any intervening insulating members. As a result, the wiring length can be minimized to provide a small size of GTO thyristor stack that can minimize the wiring inductance between a GTO thyristor and an associated diode. Further, symmetrical ballance of circuit impedance is provided.

The preferred embodiments of this invention

will now be described in conjunction with the accompanying drawings, in which:

Fig. 1 is a schematic circuit diagram of a three-phase GTO thyristor inverter to which the invention can preferably be applied;

Fig. 2 is a circuit diagram showing a connection of a one-phase component of the inverter of Fig. 1;

Fig. 3 is a plan view of a GTO thyristor stack incorporating the Fig. 2 component in accordance with one embodiment of the invention;

Fig. 4 is an electrical connection diagram of the stack of Fig. 3;

Fig. 5 is a fragmentary electrical connection diagram similar to Fig. 4 but for explaining a GTO thyristor stack in accordance with a further embodiment of the invention;

Fig. 6 is a circuit diagram of another connection of the one-phase component of the inverter of Fig. 1;

Fig. 7 is a plan view of a GTO thyristor stack incorporating the Fig. 6 component in accordance with a still further embodiment of the invention; and

Fig. 8 is an electrical connection diagram of the stack of Fig. 7.

The invention may preferably be applied to a three-phase GTO thyristor inverter as schematically shown in Fig. 1. Connected between terminals 1 and 2 of a DC power source are arms 3 to 8 each having,

as principal comp nent, GTO thyristor circuits in parallel connection. The arms are t rmed U_1 and U_2, V_1 and V_2, and W_1 and W_2 corresponding to U, V and W phases at a three-phase AC terminal 9.

Fig. 2 shows a circuit construction of a one-phase component of the inverter. A circuit of the U_1 arm 3, for example, comprises GTO thyristors 31 and 32 connected in parallel through a current balancer 33. The GTO thyristors 31 and 32 are respectively connected with diodes 34 and 35 in anti-parallel relationship and snubber capacitors 36 and 37 in parallel relationship. As well known in the art, the connection of the diodes 34 and 35 to the GTO thyristors is direct one whereas the connection of the snubber capacitors 36 and 37 to the GTO thyristors is indirect one in which a parallel connection of a diode and a resistor is usually inserted. The parallel GTO thyristor circuits are connected in series with a reactor 38 which is connected in parallel with a diode 39 and in back-to-back relationship with each of the GTO thyristors 31 and 32. The U_2 arm 4 is the same construction as the U_1 arm 3 excepting that the position of a parallel connection of a reactor 48 and a diode 49 is reversed. Although not illustrated, the components corresponding to V and W phases have each a similar circuit construction.

Fig. 3 shows one embodiment of a GTO thyristor stack in accordance with th invention, with the same elements as those in Fig. 2 designated by the same

ref rence numerals. As shown, the stack also comprises insulating plates 50 to 53, el ctrically conductive heat sinks 54 to 59, a compression spring 60, a steel ball 61, clampers 62 and 63, and connecting conductors 64 to 77.

Taking the U_1 arm 3, for instance, a pair of diodes 34 and 35 in anti-parallel connection relationship with the GTO thyristors 31 and 32 are stacked in the middle of the stack structure with the connecting conductor 73 interposed. The GTO thyristors 31 and 32 are stacked on the opposite sides of the paired diodes 34 and 35 through the intervening heat sinks 57 and 58. Thus, the diodes 34 and 35 are sandwiched by the GTO thyristors 31 and 32. The GTO thyristors 31 and 32 have outer sides electrically connected to the connecting conductors 70 and 75. These conductors are connected to the conductor 73 electrically connected in common to the diodes 34 and 35, thus constituting a point e in Fig. 2. On the outside of the conductor 75 are stacked the insulating plate 52, conductor 76, diode 39, heat sink 59 and conductor 77 in succession.

The U_2 arm 4 has the same stacking as the U_1 arm 3 with the intervening insulating plate 51, with the only exception of elimination of an insulating plate between the conductor 66 and diode 49.

Fig. 4 shows the electrical connection of the Fig. 3 stack. Points a to i in Fig. 4 respectively correspond to those in Figs. 2 and 3.

In the Fig. 3 embodiment, th stacking of th paired GTO thyristors in parallel connection and the diode associated therewith in anti-parallel relationship does not require any insulating members. Accordingly, the number of lead conductors acting as terminals can be reduced as compared with a structure requiring insulating members, and the heat sink can belong in common to adjacent elements. Thus, the stack structure can be made compact, whereby the wiring length can be decreased to minimize the wiring inductance and, at the same time, the ballance of impedance of electrical conductor wiring between two arms each having a GTO thyristor and a diode associated can be gained to get ballance of current. Also, since the central diodes are sandwiched by two GTO thyristors, the length of wirings to the snubber capacitors 36, 37 and 46, 47 of a relatively large size can be reduced as shown in Fig. 3. As previously described, the capacitor is usually connected to the GTO thyristor via a parallel connection of a diode and a resistor not shown in this figure. As a result, even if the stack structure is combined with the capacitors of large capacity in consideration of switching speed, that is, di/dt of the GTO thyristors and the heat sinks of small size that are cooled with freon, the wiring inductance can be minimized without increasing the length of wirings between the GTO thyristors and the capacitors.

Generally, the GTO thyristor element is constructed such that its thermal resistance is lower

on the anod A side than on the cathode K side so that most of generat d heat is dissipated through the anode A. The anti-parallel diode, on the other hand, has usually larger tolerance in terms of current capacity than the GTO thyristor. In other words, the GTO thyristor typically has a smaller current capacity than the packaged diode of the same size and hence it is satisfied with cooling of one side surface. In view of the above, the heat sink having one side surface in contact with the anode of the GTO thyristor and the other side surface in contact with the diode as shown in Figs. 3 and 4 succeeds in reducing itself in number.

Fig. 5 shows an electrical connection of a further embodiment of a GTO thyristor stack in accordance with the invention. As shown therein, a pair of flat type GTO thyristors may be stacked in the middle of the stack structure and sandwiched by diodes in anti-parallel connection.

Figs. 6, 7 and 8, similar to Figs. 2, 3 and 4, show a still further embodiment of a GTO thyristor stack in accordance with the invention, in which the same elements as those in Figs. 2, 3 and 4 are designated by the same reference numerals and will not be detailed.

What is different from the previous embodiment is that the position of a current balancer 43 is shifted toward a point P representative of an AC terminal. This connection permits elimination of an insulating member between a diode 39 and a GTO thyristor 31 as shown in Figs. 7 and 8.

WHAT IS CLAIMED IS

1. A gate turn-off thyristor stack comprising a pair of flat type gate turn-off thyristor elements (31, 32; 41, 42) to be connected in parallel with each other and a pair of flat type diode elements (34, 35; 44, 45) to be connected in direct parallel with the respective gate turn-off thyristor elements, wherein all the elements are stacked with electrical connection between the adjacent elements so that the elements in one of the gate turn-off thyristor element pair and the diode element pair are located opposite to each other at the middle of the stack structure and are sandwiched by the associated elements in the other pair which are provided on both sides of the stack structure, respectively, and the resulting stack structure is clamped by a pair of clamper members (62, 63).

2. A gate turn-off thyristor stack according to claim 1, wherein an electrically conductive heat dissipating member (55; 56; 57; 58) is interposed only between the gate turn-off thyristor element and the associated diode element adjacent thereto.

3. A gate turn-off thyristor stack according to claim 1, wherein said one pair located at the middle of the stack structure is the diode element pair and said other pair provided on the both sides of the stack structure is the gate turn-off thyristor element pair.

4. A gate turn-off thyristor stack according to claim 1, wherein said one pair located at the middle of

the stack structure is the gate turn-off thyristor element pair and said other pair provided on the both sides of the stack structure is the diode element pair.

5. A gate turn-off thyristor stack comprising two arms (3, 4) which are to be connected in series with each other and each of which include a pair of flat type gate turn-off thyristor elements (31, 32; 41, 42) to be connected in parallel with each other and a pair of flat type diode elements (34, 35; 44, 45) to be connected in direct parallel with the respective gate turn-off thyristor elements, wherein all the elements in each of said two arms are stacked with electrical connection between the adjacent elements so that the elements in one of the gate turn-off thyristor element pair and the diode element pair are located opposite to each other at the middle of the stack structure and are sandwiched by the associated elements in the other pair which are provided on both sides of the stack structure, respectively, said two arms each having the stack structure are integrally series-assembled with an insulating member (51) interposed therebetween, and the resulting assembly is clamped by a pair of clamper members (62, 63).

6. A gate turn-off thyristor stack according to claim 5, wherein each of said two arms includes other semiconductor element (39; 49) and said two arms are integrally series-assembled including the respective other semiconductor elements.

7. A gate turn-off thyristor stack according to claim 5, wherein an electrically conductive heat dissipating element (55; 56; 57; 58) is disposed only on one side surface of the gate turn-off thyristor element.

FIG. 1

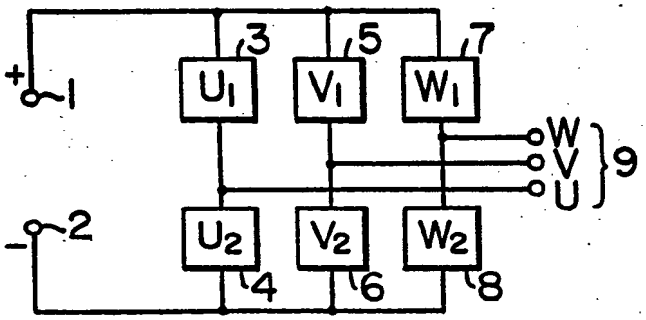


FIG. 2

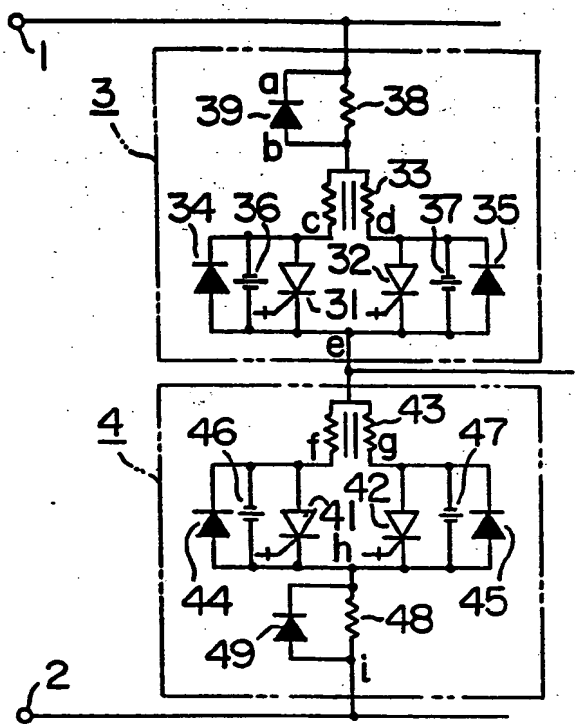


FIG. 3

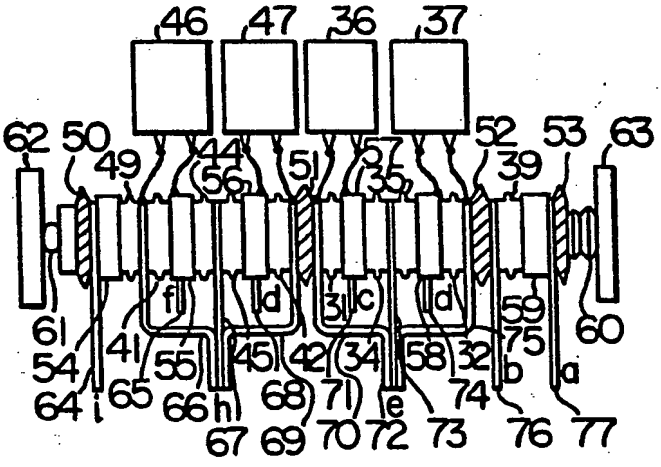


FIG. 4

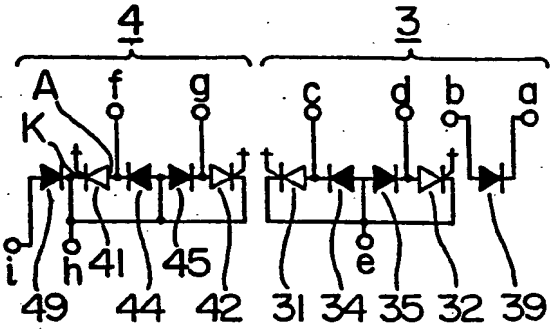


FIG. 5

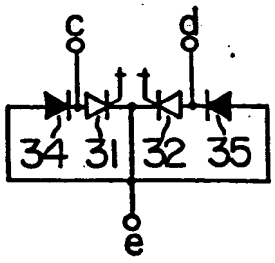


FIG. 6

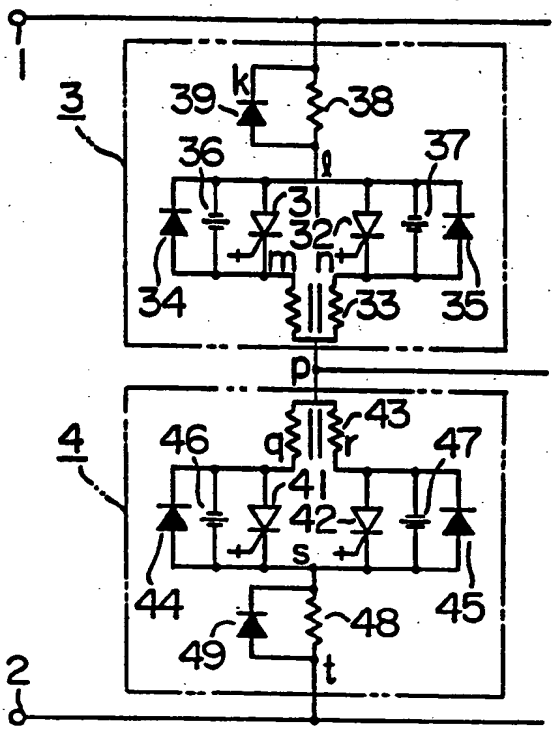


FIG. 7

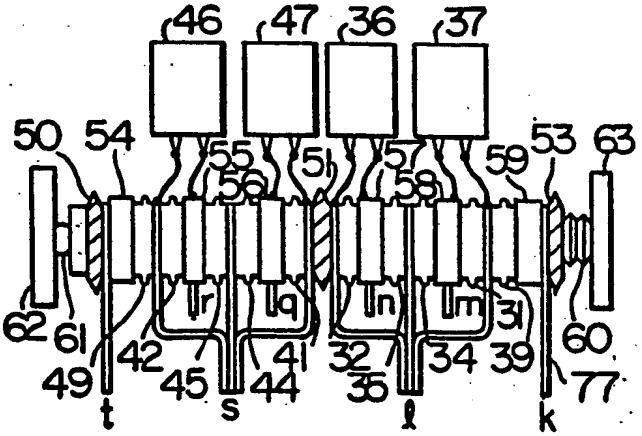
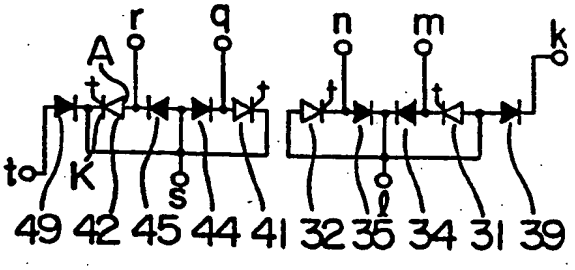


FIG. 8



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EUROPEAN SEARCH REPORT

0069971
Application number
EP 82 10 6030.8

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim
A	US - A - 3 943 426 (G. THIELE et al.) * abstract; column 2, lines 12 to 53; fig. 1 *	1,2
A	US - A - 3 573 574 (R.O. DAVIS) * column 1, line 21 to column 2, line 47; fig. 1, 4 *	1
A	US - A - 3 753 052 (D.B. ROSSER)	
A	DE - A1 - 2 838 412 (R. BOSCH) & GB - A - 2 014 360	

CLASSIFICATION OF THE APPLICATION (Int. Cl. ³)

H 02 M 1/00
H 02 M 7/46
H 01 L 25/08

TECHNICAL FIELDS SEARCHED (Int.Cl. ³)

H 01 L 23/48
H 01 L 25/08
H 02 M 1/00
H 02 M 7/00

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Place of search	Date of completion of the search	Examiner
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